Appl. No. 09/676,311
Amdt. dated September 23, 2003
Reply to Office Action of June 23, 2003

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended):

A method of handling memory errors comprising:

receiving and retaining control of a machine from an executing program after ~~a memory fault indication that is true if~~ an error in ~~the~~ a memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively; ~~and~~

reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected;

if the ~~memory~~ fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned value from the memory is invalid; and, ~~invalid,~~

returning control of the machine to the executing program.

~~otherwise,~~

~~performing error recovery.~~

2. (original):

The method of claim 1, wherein the error indication is a flag bit associated with the returned value.

3. (original):

The method of claim 1, wherein the error indication is setting the returned value to an invalid value.

4.-5. (canceled)

6. (currently amended):

A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving and retaining control of a machine from an executing program after ~~a memory fault indication that is true if~~ an error in ~~the~~ a memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively; ~~and~~

reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected;

if the ~~memory~~ fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned value from the memory is invalid; and, ~~invalid,~~

returning control of the machine to the executing program.

~~otherwise,~~

~~performing error recovery.~~

7. (original):

The machine-readable medium of claim 6, wherein the error indication is a flag bit associated with the returned value.

8. (original):

The machine-readable medium of claim 6, wherein the error indication is setting the returned value to an invalid value.

9.-10. (canceled)

11. (currently amended):

A machine comprising:

an interface to receive a value from a memory coupled to the machine;

~~a memory fault indicator that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;~~

a speculative load indicator that is true if the memory load request was issued speculatively; and

a fault deferral indicator that is true if faults can be deferred, the fault deferral indicator being set before the error in the memory is detected;

a machine-readable medium that provides instructions, which when executed by ~~a~~ the machine, cause the machine to perform operations including

receiving and retaining control of the machine from an executing program after an error in the memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory;

if the ~~memory~~ fault deferral indicator is true and the speculative load indicator is true,

providing an error indication that the returned value is invalid; and, ~~invalid,~~

returning control of the machine to the executing program.

~~otherwise,~~

~~performing error recovery.~~

12. (original):

The machine of claim 11, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

13. (original):

The machine of claim 11, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

14.-15. (canceled)

16. (currently amended):

A system comprising:

a machine;

a memory coupled to the machine; and

a machine-readable medium that provides instructions, which when executed by the machine, cause the machine to perform operations including

receiving and retaining control of the machine from an executing program after ~~a memory fault indication that is true if~~ an error in the memory is detected while executing a memory load request issued by the executing program to retrieve a value from the memory,

reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected;

receiving a speculative load indication that is true if the memory load request was issued speculatively, ~~and~~

if the ~~memory~~ fault deferral indication is true and the speculative load indication is true, providing an error indication that the returned value from the memory is invalid; and, ~~invalid,~~

returning control of the machine to the executing program.

~~otherwise,~~

~~performing error recovery.~~

17. (original):

The system of claim 16, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

18. (original):

The system of claim 16, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

19.-20. (canceled)